CURRENT LIMITER FOR MAGNETO-RESISTIVE CIRCUIT ELEMENT

Background of the Invention

Field of the Invention

This invention relates generally to circuitry for protecting an electrical circuit element from possible catastrophic damage during operation and more particularly to limiting circuitry for current in the magneto-resistive element of a magnetic read head in response to an abnormal operating condition such as a short circuit occurring in the element.

Description of Related Art

Apparatus for controlling the bias current in a magneto-resistive element utilized in a read head of a high performance hard disk drive differential preamplifier is generally known. Conventional approaches sometimes resort to fixed level limiting which wastes power consumption particularly when the bias current must be programmable over a wide range. However, such apparatus is not known to include means for limiting the current to a level which can prevent catastrophic damage when the element is shorted. Furthermore, limiting by means of shunting the excess current away requires large output devices and wastes unnecessary power.

Summary

Accordingly, it is an object of the present invention to provide apparatus for limiting the current flow therein to a desired level.

It is another object of the invention to provide apparatus for limiting the current flow in a circuit element to a desired level for damage prevention purposes.

And it is yet another object of the present invention to limit the current in a magneto-resistive element to a desired level so as to prevent catastrophic damage.

It is still a further object of the invention to provide apparatus for controlling the bias current of a magneto-resistive element used in a magnetic read head in a high performance hard disk drive differential preamplifier in the event of an abnormal condition such as a short circuit.

These and other objectives are achieved by apparatus for limiting current in an electrical circuit element, comprising: a circuit element operating in response to a bias current fed thereto for generating a voltage signal across the circuit element; a first circuit connected to one end of the circuit element for applying a bias current of a desired value to the circuit element in response to the value to an input signal; a second circuit connected to the other end of the circuit element for setting the amplitude of the voltage signal generated across the circuit element in response to the bias current; and, a third electrical circuit connected to both the first and second circuits for limiting the value of bias current to a predetermined level for an abnormal event such as a current surge, short circuit, or any other type of undesired current condition in a circuit element such as the magneto-resistive portion of a read head forming a portion of a hard disk drive.

Further scope of applicability of the present invention will become apparent from the detailed description provided hereinafter. It should be understood, however, that the detailed description and specific embodiment of the invention, while indicating the preferred embodiment thereof, it is provided by way of illustration only, since various changes,

modifications, and alterations coming within the spirit and scope of the invention will become apparent to those skilled in the art.

Detailed Description of the Drawings

The present invention will become more fully understood when the detailed description provided hereinafter is considered in connection with the accompanying drawings which are provided by way of illustration only, and thus are not meant to be considered in a limiting sense, and, wherein:

Figure 1 is a schematic electrical diagram of conventional apparatus for supplying DC bias current in a magneto-resistive head of a hard disk drive;

Figure 2 is an electrical schematic diagram in accordance with the subject invention illustrative of an apparatus for providing a DC bias current as shown in Figure 1, but now including current limiting so as to provide protection for a shorted head of a magneto-resistive read head; and,

Figure 3 is a graphical illustration of the operation of the circuitry shown in Figures 1 and 2 upon the occurrence of a short circuit event.

Detailed Description of the Invention

Referring now to the drawings wherein like reference numerals refer to like components throughout, attention is directed first to Figure 1 wherein there is shown a schematic diagram of a conventional circuit for supplying and controlling bias current to a magneto-resistive read head (MR-HEAD) 10 which is connected to a high performance hard disk drive differential preamplifier, not shown, via differential voltage Vrmr + and Vrmr - output terminals 12 and 14. The MR-HEAD 10 is comprised of resistive Rmr element 16, a series inductive Lmr element 18 and a parallel capacitive Cmr element 20. The lower and upper ends of the

read head 10 are connected to servo loops 22 and 24 which have a Vee (-5Vdc) supply voltage and Vcc (+5Vdc) supply voltage coupled thereto via terminals 26 and 28.

The lower servo loop 22 includes an OA1 operational amplifier 30, an n-p-n bipolar transistor 32, an R1 resistor 34 and an R2 resistor 36. The (+) input terminal of OA1 30 is connected to an input terminal 38 which receives a current Idac which is the output of a programmable digital-to-analog converter (DAC), not shown. The R1 resistor 34 is connected between the (+) input terminal of OA1 30 and the Vee supply terminal 26. The output terminal (OUT) of OA 30 is connected to the base of Q1 transistor 32. The emitter of Q1 transistor 32 is connected back to the (-) input terminal of OA1 30, via circuit lead 35, forming a unity gain amplifier thereby, and to an R2 resistor 36 which is also connected to the Vee supply terminal 26. OA1 30 also includes a (+) bias terminal connected to ground terminal 40 by means of circuit lead 42. The OA1 30 also includes a (-) bias terminal connected to the Vee supply terminal 28 via circuit lead 44. The collector of Q1 transistor 32 is connected to one side of the MR HEAD 10 which is common to the Vrmr - voltage output terminal 14 and to a R4 resistor 48 which connects to a circuit node 50, which also includes a connection to the upper servo loop 24 via R5 resistor 52.

The upper servo loop 24 as shown in Figure 1, in addition to R5 transistor 52, includes OA2 54, p-n-p bipolar transistor 56, and R3 resistor 58. Further as shown, the (+) input terminal of OA2 54 is connected to the circuit node 50 via circuit lead 60 while the (-) input terminal is returned to ground potential via circuit lead 62. Vcc supply potential is also connected to the (+) bias terminal of OA2 by means of circuit lead 64, while the (-) bias terminal thereof is also connected to

ground via circuit lead 66. The output terminal (Out) of OA2 54 is connected to the base of Q2 transistor 56 whose collector is commonly connected to the opposite end of the MR HEAD 10 at circuit node 68 and which is common to the Vrmr+ voltage output terminal 12 and R5 resistor 52. The emitter of Q2 transistor 56 is connected to Vcc supply potential via R3 resistor 58.

Considering now the operation of the circuit shown in Figure 1, in the quiescent or idle state where Idac at terminal 38 is zero, for example, 0mA, both inputs (+) and (-) of OA1 30 are at a potential of Vee(-5 Vdc) by virtue of R1 and R2 transistors 36 and 38. The Q1 transistor 32 is non-conducting and therefore in an OFF state. This results in a zero bias current (Ibias = 0) at the collector of Q1 transistor 32 and the voltage Vpg being greater than ground potential. Since the (+) input terminal of OA2 is tied to Vpg, the output of OA2 54 is at Vcc(+5Vdc) and since the OUT terminal of OA2 is connected to the base of Q2 transistor 56, it also is in a non-conductive or OFF state.

During normal operation, when the input current Idac > 0, the voltage at the base of Q1 transistor 32 causes it to become conductive. A current of Ibias results having a value of Idac times the value of the ratio of R1 resistor 36 and R2 resistor 38, i.e., Ibias = Idac R1/R2. This pulls the Vpg voltage at node 50 below ground potential. This causes the output of the OA2 54 applied to base Q2 transistor 56 to turn Q2 transistor 56 ON regulating the voltage at the base of Q2 to a value of Vcc - (Ibias x R3)- VbeQ2, where VbeQ2 is the base to emitter voltage of Q2. This sets the differential voltage bias Vrmr+ and Vrmr- across the MR HEAD 10 and 14 to be equal to Ibias x (Rmr/2). In a typical application, the value of Ibias in such a circuit configuration would be 4mA.

In the event that the MR HEAD 10 becomes shorted to ground while a Idac is present at terminal 38, a bias current Ibias = (Idac R1)/R2 will still be present at circuit node 46 and the voltage Vpg at circuit node 50 is still below ground potential. This causes the voltage at the base of Q2 transistor 56 to saturate to a value of VsatOA2 = Vcc - (Ishort x R3) - VbeQ2, where Ishort = (Vcc - VbeQ2 - VsatOA2)/R3. and where VsatOA2 is the saturated output voltage of OA2 54.

In normal operation, there is a balanced Ibias current in the lower and upper servo loops 22 and 24 such that the current through Q1 transistor 32, is equal to the current through Q2 transistor 56. This is depicted as the horizontal 4mA current portion 68 of the current vs. time characteristic curve 70 shown in Figure 3. However, a shorted condition in the circuit shown in Figure 1 results in the current typically rising to a Ishort value of 38mA as shown by the horizontal portion 72 of the curve 70.

Considering now the subject invention and its preferred embodiment, Figure 2 is illustrative of an arrangement which will limit the current through a magneto-resistance circuit element such as the MR HEAD 10 in the event that an abnormal current condition such as when a short occurs and until the shorted condition is removed, thereby enabling automatic recovery against any temporary shorted condition or after a head replacement because of a permanent shorted condition. The present invention is not meant to be limited to these types of events, since it could also be used for protection against undesired current surges or the like or any other type of potentially harmful current condition.

The circuit configuration of Figure 2 involves the addition of a current limiter in the form of a third servo loop 72 including not only

existing Q2 transistor 56 and R3 resistor 58, but also now OA3 74, Q3 transistor 76, R6 resistor 78, Q4 transistor 80, and R7 resistor 82. The R6 resistor 78 connects the emitter of Q3 transistor 76 to the Vee supply potential applied to terminal 28. The OUT terminal of OA1 is now connected to both the base of Q1 transistor 32 and the base of Q3 transistor 76. The base and collector of Q4 transistor 80 are connected together to R7 resistor 82 which in turn is commonly connected to the collector of Q3 transistor 76 via circuit lead 84 and to the (+) input of OA3 74 via circuit lead 86. The output terminal Out of OA3 74 is connected not only back to the (-) input thereof via circuit lead 88, but, more importantly, to the base of Q2 transistor 56 via circuit lead 90. The output of OA2 54 is also connected to the base of Q2 transistor 56 via circuit lead 92 as in the circuit of Figure 1. Thus, the outputs of OA2 54 and OA3 74 are connected in parallel to the base of Q2 transistor 56. The latter comprises an important circuit element as will now become evident. It should be noted that in the preferred embodiment of the invention as shown in Figure 2, OA2 and OA3 are operational transconductance amplifiers.

At rest or in an idle state where Idac is 0, both Q1 transistor 32 and Q3 transistor 76 are in a non-conductive state. This results in zero (Ibias=0) collector currents of Q1 and Q3 transistors 32 and 76. The OUT output terminal of OA2 connected to the base of Q2 transistor 54 is at Vcc, but the base of Q2 is also connected in parallel to the output of OA3 74 whose output is equal to Vcc - Vbe of Q4 transistor 78. This is less than the output of OA2 54. Therefore, the voltage at base of Q2 transistor 56 is at a voltage Vcc, causing it to be non-conducting.

In normal operation, when Idac > 0, a voltage is generated across R1 resistor 34 which is applied to the (+) input of OA1 30, Q1 transistor

32 now becomes conductive, causing an Ibias collector current of (Idac x R1)/R2 to flow, which pulls the voltage Vpg at circuit node 50 below ground as in Figure 1. This also causes the voltage at the OUT terminal of OA2 54 to become equal to Vcc - Vbe Q2 - (Ibias x R3). Again, noting that the output of terminal OUT of OA3 74 is in parallel with the OUT terminal of OA2 and is equal to Vcc - Vbe Q4 - (Ibias x R7). By setting a value of R7 transistor 82 equal to mR3, where m > 1, the output voltage of OA2 54 is greater than the output voltage of the OA3 74. Therefore, the voltage at the base of Q2 transistor 56 sees the output of OA2 54 and thus a normal operation as in Figure 1 is obtained.

However, when the MR HEAD 10 becomes shorted to ground, even though the Vpg voltage at circuit node 50 is still below ground, the voltage at the base of Q2 transistor 56 will become clamped to the output voltage of the OA3 74, which is greater than VsatOA2. Accordingly, the voltage at the base of Q2 transistor 56 is regulated to a value of Vcc - Ishort x R3 - VbeQ2, where I short = m x Ibias where m is equal to R7/R3. The value of R7 resistor 82 is selected to be greater than that of R3 resistor 58 so that m>1. Such an operation is shown by the waveform 74 in Figure 3 where a shorted condition occurs at 5μs and the Ishort portion 76 is clamped to 4.4mA where, for example, the values of R7 = 110 ohms and the value of R3 = 100 ohms, then m = 110/100 = 1.1 and an Ishort of 4.4mA results for an Ibias of 4.0mA.

The embodiment of the subject invention as shown in Figure 2 is adaptive in that Ishort will be limited to m x Ibias for the entire range of Ibias. Also, in this embodiment power is not wasted by shunting the excess current to ground.

While the subject invention was developed specifically for controlling the bias current of a magneto-resistive read head which is

used in a hard disk drive, the basic principle can be applied to any application requiring a limiting of DC current to a desired level. Also, while bipolar transistors are shown in the disclosed embodiment of the invention, other types of semiconductor devices could be employed such as field effect transistors, for example. Furthermore, the subject invention can be implemented in the structure of an integrated circuit.

The foregoing detailed description merely illustrates the principles of the invention. It will thus be appreciated that those skilled in the art will be able to devise various arrangements which, although not explicitly described or shown herein, embody the principles of the invention and thus are within its spirit and scope.